In the Claims

Please cancel claims 1-35 and enter new claims 36-49.

Claims 1-35 (Canceled)

36. (New) An apparatus for delaying an audio signal comprising:

a first FIFO register receptive to a digital audio signal;

an audio format detection coupled to the first FIFO register and operative to detect a format of the digital audio signal;

a memory controller coupled to the FIFO register;

a memory chip coupled to the memory controller;

a write address generator coupled to the audio format detection and memory controller;

a read address generator coupled to the memory controller; and

a second FIFO register coupled to the memory controller and operative to provide a time delay in the digital audio signal the duration of which is related to the detected format of the digital audio signal.

37. (New) The apparatus as claimed in claim 36, wherein the digital audio signal further comprises a serial audio clock signal and a plurality of accompanying signals.

38. (New) The apparatus as claimed in claim 37, wherein the accompanying signals further comprises a data signal and a frame synchronization signal.

39. (Original) The apparatus as claimed in claim 37, wherein the audio format detection is operable to detect a number of edge transitions in the serial audio clock signal and provide a corresponding detected count.

40. (New) The apparatus claimed in claim 37, wherein the audio format detection further comprises a plurality of model data, wherein each model data represents one of a plurality of audio signal formats and a corresponding one of a plurality of time delay data, wherein the detected count is compared to the model data, the audio format detection operable to provide the delay data representing the model data that is equal to the detected count.

41. (New) The apparatus as claimed in claim 40, wherein the processed clock signal is synchronized to a reference clock.

42. (New) The apparatus as claimed in claim 37, wherein the audio format detection is operable to provide a processed clock signal by dividing the serial clock signal by a constant.

43. (New) The apparatus according to claim 42, wherein the processing is operable to compare a new time delay data to an old time delay data, the processing device operable to reconfigure a buffer if the new time delay data is not equal to the old time delay data.

44. (New) The apparatus as claimed in claim 40, wherein the detected count is compared to the model data by a plurality of comparators.

45. (New) The apparatus as claimed in claim 40, wherein the provided time delay data is a first offset value, the processing device operable to resize a write address pointer with the offset value.

46. (New) The apparatus as claimed in claim 40, wherein the provided time delay data is a second offset value, the processing device operable to resize a read address pointer with the offset value.

47. (New) The apparatus as claimed in claim 40, wherein the processing device further comprises a memory unit to provide the time delay corresponding to the time delay data.

48. (New) The apparatus as claimed in claim 45, wherein the processing device further comprises a first parameter and a second parameter, the first parameter configured accordingly to the provided time delay data.

49. (New) The apparatus as claimed in claim 48, wherein the first parameter is a write address parameter, the second parameter is a read address parameter, and the memory unit is a buffer.